U.S.C. §103(a) as being unpatentable over Park et al. (US 5,296,400) in view of Poppert et al. (US 4,593,459); (2) rejected claims 22, 24, 25, 28, 29, and 32-37 under U.S.C. §103(a) as being unpatentable over Noguchi et al. (US 4,935,802) in view of Poppert et al. (US 4,593,459). Applicants respectfully request reconsideration of the application in view of the foregoing amendments and the following remarks.

Applicants wish to thank the Examiner for his time in discussing the application on August 14, 2002. Applicants have added the limitation of a silicide layer to claims 22 and 26 following Examiner's suggestion that this addition appears to distinguish Applicant's invention over the prior art of record.

Some of the technical differences between the applied references and various embodiments of the invention will now be discussed. Of course, these discussed differences, which are disclosed in detail in the patent specification, do not define the scope or interpretation of any of the claims. Where presented below, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Applicants teach trench isolation structures on microelectronic devices and methods for forming the same. In one embodiment, a microelectronic device includes a microelectronic substrate having an upper surface. The device further includes a gate structure, including a gate oxide layer formed on the upper surface of the substrate, a first gate layer formed on the gate oxide layer, an adhesion layer formed on the first gate layer, and a conductive silicide layer formed on the adhesion layer. The gate structure has a trench at least partially disposed therein extending into the substrate substantially perpendicularly to the upper surface of the substrate. A field oxide layer is disposed at least partially in the trench. The field oxide layer has sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide layer. The substantially straight sides do not contact the gate oxide layer. Further, the substantially straight sides extend upwardly from the trench substantially perpendicularly to the upper surface of the substrate and past the upper surface of the substrate above adjacent structures on the upper surface of the substrate. The substantially straight sides do not extend laterally from the trench over the upper surface of the substrate. The top surface of the field oxide layer is between the level of the upper surface of the substrate and the level of an

upper surface of the first gate layer. In one aspect, the silicide layer comprises tungsten silicide. In another aspect, a thin layer of oxide is formed on the silicide layer.

In another embodiment a microelectronic device includes a silicon substrate having a trench formed in a surface thereof. The trench extends into the substrate substantially perpendicularly to the surface of the substrate and is bounded on all sides by the substrate. A field oxide is disposed in the trench. The field oxide has sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide. The substantially straight sides project outwardly from the trench beyond the surface of the substrate, and beyond any adjacent structures on the surface of the substrate, substantially perpendicularly to the surface of the substrate and do not extend laterally from the trench over the surface of the substrate. A component is formed on the field oxide, The component extends from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate. The component comprises an adhesion layer formed on the field oxide and a conductive silicide layer formed on the adhesion layer.

Because the height of the field oxide "isolation pad" is reduced compared with the height of the component, an edge spacer that may otherwise form along the edges of the isolation pad is reduced or eliminated. Therefore the isolation pad advantageously requires less surface area on the apparatus.

Park et al.

Park et al. (U.S. 5,296,400) teaches methods of manufacturing semiconductor devices. As best shown in Figure 1A, Park et al. teaches a semiconductor device including a substrate 1, a transistor having a gate oxide layer 4 formed on the substrate 1, and a gate electrode 5 formed on the gate oxide layer 4. (2:60-65). A mask oxide 6 is formed on the gate electrode 5, and a first insulating layer 7 (for example an oxide layer) is formed over the top of the entire structure. (2:62-65). Park et al. further teaches a field oxide layer 3 formed in the substrate 1. (2:60-65). As best shown in Figure 1A of Park et al., the field oxide layer 3 has a rounded "bird's beak" shape typical of LOCOS methods.

Park et al. does not teach or suggest the microelectronics structures taught by Applicants. Specifically, Park et al. does not teach, disclose or fairly suggest a conductive

silicide layer formed on the adhesion layer. Rather, Park et al. teaches a gate oxide layer 4 formed on the substrate 1, a gate electrode 5 formed on the gate oxide layer 4, a mask oxide 6 formed on the gate electrode 50, and a first insulating layer 7 formed on the mask oxide 6.

Moreover, Park et al. does not teach, disclose or fairly or suggest the field oxide layer having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide layer, the substantially straight sides not contacting the gate oxide layer, the substantially straight sides extending upwardly from the trench substantially perpendicularly to the upper surface of the substrate and past the upper surface of the substrate above adjacent structures on the upper surface of the substrate, the substantially straight sides not extending laterally from the trench over the upper surface of the substrate, the top surface of the field oxide layer being between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer. Rather, Park et al. teaches a field oxide layer 3 having a rounded "bird's beak" shape. Because Park et al. teaches that the field oxide layer 3 is formed using a LOCOS process, there is no trench formed in the substrate that is filled with field oxide, as taught by Applicants. Furthermore, the "bird's beak" shape taught by Park et al. takes up more space than the field oxide layer taught by Applicants. Thus the field oxide layer taught by Park et al. restricts the miniaturization realizable in a microelectronic device more severely than does the field oxide layer taught by Applicants. For these reasons, Park et al. does not disclose, teach or fairly suggest the structures taught by Applicants.

Poppert et al.

Poppert et al. (U.S. 4,593,459) teaches substrates for the fabrication of semiconductor integrated circuit devices therein. As best shown in Figures 7 and 8, Poppert et al. teaches a monolithic integrated circuit structure including low resistivity polycrystalline silicon gate members 53, 54 formed on gate insulating layers 51, 52, respectively. (5:24-32). Poppert et al. further teaches a silicon dioxide region 48 formed in a trench 46 with silicon dioxide portions 40 formed on opposite sides thereof. (5:13-15). The silicon dioxide portions 40 extend from the silicon dioxide region 48 outwardly over the edges of the trench 46, and are adjacent to and in contact with the gate insulating layers 51, 52. (5:13-46). As best shown in Figure 8, the silicon dioxide region 48 extends upwardly from the surface of the substrate to a level that is approximately equal to the upper surface of the gate members 53, 54, while the

silicon dioxide portions 40 extend to levels that are higher than the upper surfaces of the gate members 53, 54.

Poppert et al. does not remedy the above-noted absent teachings of Park et al., and does not disclose, teach or fairly suggest the microelectronics structures taught by Applicants. Specifically, Poppert et al. does not teach or suggest a conductive silicide layer formed on the adhesion layer. Rather, Poppert et al. teaches polycrystalline silicon gate members 53, 54 formed on gate insulating members 51, 52.

Moreover, Park et al. does not teach, disclose or fairly or suggest the field oxide layer having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide layer, the substantially straight sides not contacting the gate oxide layer, the substantially straight sides extending upwardly from the trench substantially perpendicularly to the upper surface of the substrate and past the upper surface of the substrate above adjacent structures on the upper surface of the substrate, the substantially straight sides not extending laterally from the trench over the upper surface of the substrate, the top surface of the field oxide layer being between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer. According to the teachings of Poppert et al., silicon dioxide portions 40 are engaged with the silicon dioxide region 48 and extend outwardly over the sides of the trench 46. In addition, the silicon dioxide region 48 taught by Poppert does not extend above the adjacent silicon dioxide portions 40, but rather, as shown in Figure 8, the adjacent silicon dioxide portions 40 of Poppert extend above the silicon dioxide region 48. Therefore, Poppert et al. teaches away from Applicants' novel structures which include a field oxide layer with straight side walls that do not extend laterally from the trench over the upper surface of the substrate.

Furthermore, the field oxide portions 40 taught by Poppert et al. are in contact with the gate insulating layers 51, 52 of the gate structures. For this additional reason, Poppert et al. teaches away from the novel microelectronics structures taught by Applicants in which the field oxide layer does not contact the gate oxide layers of the local gate structures.

Additionally, the silicon dioxide portions 40 of Poppert et al. extend upwardly to a level that is greater than the level of the upper surface of the gate members 53, 54. For this additional reason, Poppert et al. teaches away from the structures taught by Applicants, which

require that the top surface of the field oxide layer be between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer.

Thus, while the combination of Park et al. in view of Poppert et al. fails to teach or suggest Applicants' inventive structures, Applicants respectfully submit that there is also no motivation to combine the teachings of Park et al. with the teachings of Poppert et al.. The mere fact that references can be combined does not render the resultant combination obvious unless the prior art also objectively suggests the desirability of the resulting combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); *In re Kotzab*, 217 F.3d 1365, 55 U.S.P.Q.2d 1313 (Fed. Cir. 2000). Park et al. teaches a conventional LOCOS process that produces the familiar "birds beak" field oxide shape and does not involve forming a trench in a substrate. On the other hand, Poppert et al. teaches the opposing approach of using a trench isolation process. Since trench isolation processes are substantially different than conventional LOCOS processes, there is no motivation to combine the teachings of Poppert et al. with the teachings of Park et al.. Furthermore, because Poppert et al. teaches away from structures wherein the field oxide layer (1) extends above adjacent structures; (2) does not extend laterally from the trench over the upper surface of the substrate; (3) does not contact the gate oxide layers of the local gate structures; and (4) the top surface of the field oxide layer is between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer, there is no motivation to combine the teachings of Poppert et al. with the teachings of Park et al. to arrive at Applicants' invention. Thus, Applicants respectfully submit that the combination of these references is the result of impermissible hindsight analysis.

Noguchi et al.

Noguchi et al. (U.S. 4,935,802) teaches methods of manufacturing semiconductor devices. As best shown in Figure 2, Noguchi et al. teaches a semiconductor device including a P-type substrate 5 and a transistor 20 having an SiO_2 gate layer 2 formed on the substrate 5 and a metallic gate electrode 3, such as poly Si, formed on the gate layer 2. (3:43-67). Noguchi et al. also teaches a memory cell transistor 10 formed in the substrate 5, comprising a first gate insulating layer 2a, a floating electrode 3a, a second insulating layer 2b and a control electrode 3b. (3:58-65). Noguchi et al. further teaches a field insulating layer 4 formed in the substrate 5 by a conventional LOCOS method. (4:24-26).

Noguchi et al. does not remedy the above-noted deficiencies in the teachings of Park et al. and Poppert et al.. Specifically, Noguchi et al. does not disclose, teach or fairly suggest a conductive silicide layer formed on the adhesion layer. Rather, Noguchi et al. teaches a transistor 20 having an SiO_2 gate layer 2 formed on the substrate 5 and a metallic gate electrode 3, such as poly Si, formed on the gate layer 2.

Moreover, Noguchi et al. does not disclose, teach or fairly suggest the field oxide layer having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide layer, the substantially straight sides not contacting the gate oxide layer, the substantially straight sides extending upwardly from the trench substantially perpendicularly to the upper surface of the substrate and past the upper surface of the substrate above adjacent structures on the upper surface of the substrate, the substantially straight sides not extending laterally from the trench over the upper surface of the substrate, the top surface of the field oxide layer being between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer. According to Noguchi et al., the sides of the field insulating layer 4 are not substantially parallel from a bottom of the trench to a top surface of the field oxide. Nor do they extend upwardly from the trench substantially perpendicularly to the upper surface of the substrate and past the upper surface of the substrate. Rather, the field insulating layer 4 of Noguchi et al. exhibits the generally rounded or "bird's beak" shape typical of conventional LOCOS processes. Furthermore, because Noguchi et al. teaches that the field insulating layer 4 is formed using a LOCOS process, there is no trench formed in the substrate that is filled with field oxide, as taught by Applicants. For this additional reason, Noguchi et al. does not teach or suggest the structures taught by Applicants.

Again, as with Park et al., there is no motivation to combine the teachings of Noguchi et al. with the teachings of Poppert et al.. As stated above, the mere fact that references can be combined does not render the resultant combination obvious unless the prior art also objectively suggests the desirability of the resulting combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); *In re Kotzab*, 217 F.3d 1365, 55 U.S.P.Q.2d 1313 (Fed. Cir. 2000). Noguchi et al. involves a conventional LOCOS process that does not involve forming a trench in a substrate and produces the familiar "birds beak" field oxide shape. In contrast, Poppert et al. teaches the opposing approach of using a trench isolation process. Since trench

isolation processes are substantially different than conventional LOCOS processes, there is no motivation to combine the teachings of Poppert et al. with the teachings of Noguchi et al.. Furthermore, because Poppert et al. teaches away from structures wherein the field oxide layer (1) extends above adjacent structures; (2) does not extend laterally from the trench over the upper surface of the substrate; (3) does not contact the gate oxide layers of the local gate structures; and (4) the top surface of the field oxide layer is between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer, there is no motivation to combine the teachings of Poppert et al. with the teachings of Noguchi et al. to arrive at Applicants' invention. Thus, Applicants respectfully submit that the combination of these references is the result of impermissible hindsight analysis.

I. *Rejected claims 22 and 24-37 under 35 U.S.C. § 103(a) as being unpatentable over Park et al. (US 5,296,400, of record) in view of Poppert et al. (US 4,593,459, of record); Rejected claims 22, 24, 25, 28, 29, and 32-37 under U.S.C. § 103(a) as being unpatentable over Noguchi et al. (US 4,935,802, of record) in view of Popper et al. (US 4,593,459, of record).*

Claims 22, 24-25, 35-37 and New Claim 38

Amended claim 22 recites a microelectronic device comprising a microelectronic substrate having an upper surface, a gate structure including a gate oxide layer formed on the upper surface of the substrate, a first gate layer formed on the gate oxide layer, an adhesion layer formed on the first gate layer, *and a conductive silicide layer formed on the adhesion layer*, the gate structure having a trench at least partially disposed therein and extending into the substrate substantially perpendicularly to the upper surface of the substrate, and *a field oxide layer at least partially in the trench, the field oxide layer having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide layer, the substantially straight sides not contacting the gate oxide layer, the substantially straight sides extending upwardly from the trench substantially perpendicularly to the upper surface of the substrate* and past the upper surface of the substrate above adjacent structures on the upper surface of the substrate, *the substantially straight sides not extending laterally from the trench*

over the upper surface of the substrate, the top surface of the field oxide layer being between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer. (emphasis added).

As described more fully above, the combination of Park et al., Poppert et al, and Noguchi et al. does not disclose, teach, or fairly suggest the microelectronic device as disclosed in claim 22. Specifically, neither Park et al., Poppert et al, nor Noguchi et al., singly or in combination, teach or suggest a conductive silicide layer formed on the adhesion layer. Nor does Park et al., Poppert et al, or Noguchi et al., singly or in combination, teach or suggest a field oxide layer at least partially in the trench, the field oxide layer extending above adjacent structures and having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide layer, the substantially straight sides not contacting the gate oxide layer, the substantially straight sides extending upwardly from the trench substantially perpendicularly to the upper surface of the substrate. Furthermore, Park et al., Poppert et al, and Noguchi et al., also fail to teach or suggest the substantially straight sides not extending laterally from the trench over the upper surface of the substrate, the top surface of the field oxide layer being between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer. In addition, as discussed more fully above, there is no motivation to combine the teachings of Noguchi et al. and Park et al. with Poppert et al.. Both Noguchi et al. and Park et al. teach a conventional LOCOS process that does not involve forming a trench in a substrate and produces the familiar "birds beak" field oxide shape. Since trench isolation processes are substantially different processes from conventional LOCOS processes, there is no motivation to combine the teachings of Noguchi et al. and Park et al. with those of Poppert et al.. Therefore claim 22 is patentable over Noguchi et al., Park et al. and Poppert et al..

Claims 24-25, 35-37 and new claim 38 depend from claim 22 and are patentable over Noguchi et al., Park et al. and Poppert et al for the same reasons as claim 22 and also due to additional limitations contained in these claims. For example, amended claim 24 recites the microelectronic device of claim 22 wherein the silicide layer comprises tungsten silicide. Similarly, amended claim 25 recites the microelectronic device of claim 22, further comprising a thin layer of oxide formed on the silicide layer. Claim 35 recites the microelectronic device of claim 22 wherein the first gate layer comprises a polysilicon layer. Claim 36 recites the

microelectronic device of claim 22 wherein the field oxide level is less than or equal to approximately one half the distance between the upper surface of the substrate and the upper surface of the first gate layer. Claim 37 recites the microelectronic device of claim 24 wherein the field oxide level is less than or equal to approximately one half the distance between the upper surface of the substrate and the upper surface of the silicide layer. And new claim 38 recites the microelectronic device of claim 22 wherein a first distance measured from the top surface of the field oxide layer to the level of the upper surface of the substrate is up to one half of a second distance measured from the level of the upper surface of the substrate to the upper surface of the gate structure. For these reasons, claims 24-25, 35-37 and new claim 38 are patentable over Noguchi et al., Park et al. and Poppert et al..

Claims 26-27 and New Claims 39-41

Amended claim 26 recites a microelectronic device comprising a silicon substrate having a trench formed in a surface thereof, the trench extending into the substrate substantially perpendicularly to the surface of the substrate and being bounded on all sides by the substrate, a field oxide in the trench, *the field oxide having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the substantially straight sides projecting outwardly from the trench beyond the surface of the substrate, and beyond any adjacent structures on the surface of the substrate, substantially perpendicularly to the surface of the substrate and not extending laterally from the trench over the surface of the substrate, and a component formed on the field oxide*, the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the component comprising an adhesion layer formed on the field oxide and *a conductive silicide layer formed on the adhesion layer*. (emphasis added).

As described more fully above, the combination of Park et al., Poppert et al, and Noguchi et al. does not disclose, teach, or fairly suggest the microelectronic device as disclosed in claim 26. Specifically, neither Park et al., Poppert et al, nor Noguchi et al., singly or in combination, teach or suggest the field oxide having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the

substantially straight sides projecting outwardly from the trench beyond the surface of the substrate, and beyond any adjacent structures on the surface of the substrate, substantially perpendicularly to the surface of the substrate and not extending laterally from the trench over the surface of the substrate, and a component formed on the field oxide. Nor does Park et al., Poppert et al, or Noguchi et al., singly or in combination, teach or suggest a conductive silicide layer formed on the adhesion layer. In addition, as discussed more fully above, there is no motivation to combine the teachings of Noguchi et al. and Park et al. with Poppert et al.. Both Noguchi et al. and Park et al. teach a conventional LOCOS process that does not involve forming a trench in a substrate and produces the familiar "birds beak" field oxide shape. Since trench isolation processes are substantially different processes from conventional LOCOS processes, there is no motivation to combine the teachings of Noguchi et al. and Park et al. with those of Poppert et al.. Therefore claim 26 is patentable over Noguchi et al., Park et al. and Poppert et al..

Claims 27 and new claims 39-41 depend from claim 26 and are patentable over Noguchi et al., Park et al. and Poppert et al for the same reasons as claim 26 and also due to additional limitations contained in these claims. For example, claim 27 recites the microelectronic device of claim 26, further comprising an oxide spacer adjacent the component. Similarly, new claim 39 recites the microelectronic device of claim 26, further comprising a gate structure including a gate oxide layer formed on the upper surface of the substrate, the gate structure extending from the upper surface of the substrate to a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the field oxide not contacting any portion of the gate structure. New claim 40 recites the microelectronic device of claim 26 wherein the silicide layer comprises tungsten silicide. And new claim 41 recites the microelectronic device of claim 26, further comprising a thin layer of oxide formed on the silicide layer. For these reasons, claims 27 and new claims 39-41 are patentable over Noguchi et al., Park et al. and Poppert et al..

Claims 28-29

Amended claim 28 recites a microelectronic device comprising a microelectronic substrate having a trench formed in a surface thereof, the trench extending into the substrate substantially perpendicularly to the surface of the substrate, *a field oxide in the trench, the field*

oxide having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the substantially straight sides extending from the trench beyond the surface of the substrate and above any adjacent structures on the upper surface of the substrate, the substantially straight sides extending substantially perpendicularly to the surface of the substrate and not extending laterally from the trench over the surface of the substrate, and a gate structure formed on the substrate, the gate structure extending from the upper surface of the substrate by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the field oxide not contacting any portion of the gate structure. (emphasis added).

As described more fully above, the combination of Park et al., Poppert et al, and Noguchi et al. does not disclose, teach, or fairly suggest the microelectronic device as disclosed in claim 28. Specifically, neither Park et al., Poppert et al, nor Noguchi et al., singly or in combination, teach or suggest a field oxide in the trench, the field oxide having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the substantially straight sides extending from the trench beyond the surface of the substrate and above any adjacent structures on the upper surface of the substrate, the substantially straight sides extending substantially perpendicularly to the surface of the substrate and not extending laterally from the trench over the surface of the substrate. In addition, as discussed more fully above, there is no motivation to combine the teachings of Noguchi et al. and Park et al. with Poppert et al.. Both Noguchi et al. and Park et al. teach a conventional LOCOS process that does not involve forming a trench in a substrate and produces the familiar "birds beak" field oxide shape. Since trench isolation processes are substantially different processes from conventional LOCOS processes, there is no motivation to combine the teachings of Noguchi et al. and Park et al. with those of Poppert et al.. Therefore claim 28 is patentable over Noguchi et al., Park et al. and Poppert et al..

Claim 29 depends from claim 28 and is patentable over Noguchi et al., Park et al. and Poppert et al for the same reasons as claim 28 and also due to additional limitations contained in these claims. For example, claim 29 recites the microelectronic device of claim 28, further comprising an oxide spacer adjacent the gate structure. For these reasons, claim 29 is patentable over Noguchi et al., Park et al. and Poppert et al..

Claims 30-31 and New Claim 42

Amended claim 30 recites a microelectronic device comprising a microelectronic substrate having a recess formed in a surface thereof, the recess extending into the substrate substantially perpendicularly to the surface of the substrate, and a field oxide deposited in the recess, *the field oxide having sides that are substantially straight and substantially parallel from a bottom of the recess to a top surface of the field oxide, the substantially straight sides extending substantially perpendicularly to the surface of the substrate from the recess and beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of a component formed on the field oxide, the field oxide not extending laterally from the recess over the surface of the substrate, and the field oxide extending above adjacent structures on the upper surface of the substrate.* (emphasis added).

As described more fully above, the combination of Park et al., Poppert et al, and Noguchi et al. does not disclose, teach, or fairly suggest the microelectronic device as disclosed in claim 30. Specifically, neither Park et al., Poppert et al, nor Noguchi et al., singly or in combination, teach or suggest the field oxide having sides that are substantially straight and substantially parallel from a bottom of the recess to a top surface of the field oxide, the substantially straight sides extending substantially perpendicularly to the surface of the substrate from the recess and beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of a component formed on the field oxide, the field oxide not extending laterally from the recess over the surface of the substrate, and the field oxide extending above adjacent structures on the upper surface of the substrate. In addition, as discussed more fully above, there is no motivation to combine the teachings of Noguchi et al. and Park et al. with Poppert et al.. Both Noguchi et al. and Park et al. teach a conventional LOCOS process that does not involve forming a trench in a substrate and produces the familiar "birds beak" field oxide shape. Since trench isolation processes are substantially different processes from conventional LOCOS processes, there is no motivation to combine the teachings of Noguchi et al. and Park et al. with those of Poppert et al.. Therefore claim 30 is patentable over Noguchi et al., Park et al. and Poppert et al..

Claim 31 and new claim 42 depend from claim 30 and are patentable over Noguchi et al., Park et al. and Poppert et al for the same reasons as claim 30 and also due to additional limitations contained in these claims. For example, claim 31 recites the microelectronic device of claim 30, further comprising an oxide spacer adjacent the component. Similarly, new claim 42 recites the microelectronic device of claim 30 further comprising a gate structure including a gate oxide layer formed on the upper surface of the substrate, the gate structure extending from the upper surface of the substrate to a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the field oxide not contacting any portion of the gate structure. For these reasons, claim 31 and new claim 42 are patentable over Noguchi et al., Park et al. and Poppert et al..

Claims 32-33

Amended claim 32 recites a microelectronic device comprising a microelectronic substrate having a trench formed in a surface thereof, a gate structure formed on the substrate, the gate structure including a gate oxide layer formed on the microelectronic substrate, a first gate layer formed on the gate oxide layer, an adhesion layer formed on the first gate layer, and a conductive layer formed on the adhesion layer, and a field oxide deposited in the trench, *the field oxide extending substantially perpendicularly to the surface of the substrate from the trench beyond the surface of the substrate and above adjacent structures on the upper surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate, the field oxide having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the substantially straight sides not contacting the gate oxide layer and not extending laterally from the recess over the surface of the substrate.* (emphasis added)

As described more fully above, the combination of Park et al., Poppert et al, and Noguchi et al. does not disclose, teach, or fairly suggest the microelectronic device as disclosed in claim 32. Specifically, neither Park et al., Poppert et al, nor Noguchi et al., singly or in combination, teach or suggest the field oxide extending substantially perpendicularly to the surface of the substrate from the trench beyond the surface of the substrate and above adjacent

structures on the upper surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate, the field oxide having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the substantially straight sides not contacting the gate oxide layer and not extending laterally from the recess over the surface of the substrate. In addition, as discussed more fully above, there is no motivation to combine the teachings of Noguchi et al. and Park et al. with Poppert et al.. Both Noguchi et al. and Park et al. teach a conventional LOCOS process that does not involve forming a trench in a substrate and produces the familiar "birds beak" field oxide shape. Since trench isolation processes are substantially different processes from conventional LOCOS processes, there is no motivation to combine the teachings of Noguchi et al. and Park et al. with those of Poppert et al.. Therefore claim 32 is patentable over Noguchi et al., Park et al. and Poppert et al..

Claim 33 depends from claim 26 and is patentable over Noguchi et al., Park et al. and Poppert et al for the same reasons as claim 32 and also due to additional limitations contained in claim 33. For example, claim 33 recites the microelectronic device of claim 32, further comprising an oxide spacer adjacent the gate structure. For these reasons, claim 33 is patentable over Noguchi et al., Park et al. and Poppert et al..

Claim 34 and New Claim 43

Amended claim 34 recites a microelectronic device comprising a microelectronic substrate having a surface with a trench formed therein, *a field oxide within the trench and having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the substantially straight sides projecting therefrom substantially perpendicularly to the surface of the substrate and above adjacent structures on the upper surface of the substrate by a height which is small enough to prevent the formation of spacers adjacent the field oxide, the field oxide not extending laterally from the trench over the surface of the substrate, and a component formed on the field oxide.* (emphasis added).

As described more fully above, the combination of Park et al., Poppert et al, and Noguchi et al. does not disclose, teach, or fairly suggest the microelectronic device as disclosed in claim 34. Specifically, neither Park et al., Poppert et al, nor Noguchi et al., singly or in

combination, teach or suggest a field oxide within the trench and having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the substantially straight sides projecting therefrom substantially perpendicularly to the surface of the substrate and above adjacent structures on the upper surface of the substrate by a height which is small enough to prevent the formation of spacers adjacent the field oxide, the field oxide not extending laterally from the trench over the surface of the substrate, and a component formed on the field oxide. In addition, as discussed more fully above, there is no motivation to combine the teachings of Noguchi et al. and Park et al. with Poppert et al.. Both Noguchi et al. and Park et al. teach a conventional LOCOS process that does not involve forming a trench in a substrate and produces the familiar "birds beak" field oxide shape. Since trench isolation processes are substantially different processes from conventional LOCOS processes, there is no motivation to combine the teachings of Noguchi et al. and Park et al. with those of Poppert et al.. Therefore claim 34 is patentable over Noguchi et al., Park et al. and Poppert et al..

New claim 43 depends from claim 34 and is patentable over Noguchi et al., Park et al. and Poppert et al for the same reasons as claim 34 and also due to additional limitations contained in claim 43. For example, claim 43 recites the microelectronic device of claim 34, further comprising a gate structure including a gate oxide layer formed on the upper surface of the substrate, the gate structure extending from the upper surface of the substrate to a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the field oxide not contacting any portion of the gate structure. For these reasons, claim 43 is patentable over Noguchi et al., Park et al. and Poppert et al..

For the foregoing reasons, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 22 and 24-37 under 35 U.S.C. § 103(a) as being unpatentable over Park et al. (US 5,296,400, of record) in view of Poppert et al. (US 4,593,459, of record), and the rejection of claims 22, 24, 25, 28, 29, and 32-37 under U.S.C. § 103(a) as being unpatentable over Noguchi et al. (US 4,935,802, of record) in view of Popper et al. (US 4,593,459, of record).

CONCLUSION

In light of the foregoing amendments and remarks, Applicants believe that pending claims 22, 24-37 and new claims 38-43 are in condition for allowance, and that action is respectfully requested. In accordance with 37 CFR § 1.121, attached hereto is an attached page entitled "Version with Markings to Show Changes Made" showing the specific changes made to the claims by the current amendment. If there are any remaining matters that can be handled in a telephone conference, the Examiner is invited to telephone the undersigned attorney, Jim Patterson, at (206) 903-5498.

Respectfully submitted,
DORSEY & WHITNEY LLP

Jim Patterson
Registration No. P-52,103

JP/dms
Enclosures:
Postcard
Fee Transmittal Sheet (+ copy)
Associate Power of Attorney

1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

h:\ip\documents\clients\micron technology\00\500055.02\500055.02 amend af.doc

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend claims 22, 24-26, 28, 30, 32, 34 and add claims 38-43 as follows:

22. (Five Times Amended) A microelectronic device, comprising:

a microelectronic substrate having an upper surface;

a gate structure including a gate oxide layer formed on the upper surface of the substrate, a first gate layer formed on the gate oxide layer, [and]an adhesion layer formed on the first gate layer, and a conductive silicide layer formed on the adhesion layer, the gate structure having a trench at least partially disposed therein and extending into the substrate substantially perpendicularly to the upper surface of the substrate; and

a field oxide layer at least partially in the trench, the field oxide layer having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide layer, the substantially straight sides not contacting the gate oxide layer, the substantially straight sides[and] extending upwardly from the trench substantially perpendicularly to the upper surface of the substrate and past the upper surface of the substrate above adjacent structures on the upper surface of the substrate, the substantially straight sides [and]not extending laterally from the trench over the upper surface of the substrate, [the field oxide layer having a field oxide level]the top surface of the field oxide layer being between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer.

24. (Twice Amended) The microelectronic device of claim 22[, further comprising] wherein[a] the silicide layer [formed on the adhesion layer]comprises tungsten silicide.

25. (Twice Amended) The microelectronic device of claim 22, further comprising [a conductive layer formed on the adhesion layer] a thin layer of oxide formed on the silicide layer.

26. (Four Times Amended) A microelectronic device, comprising:

a [microelectronic]silicon substrate having a trench formed in a surface thereof, the trench extending into the substrate substantially perpendicularly to the surface of the substrate and being bounded on all sides by the substrate;

a field oxide in the trench, the field oxide having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the substantially straight sides projecting outwardly from the trench beyond the surface of the substrate, and beyond any adjacent structures on the surface of the substrate, substantially perpendicularly to the surface of the substrate and not extending laterally from the trench over the surface of the substrate; and

a component formed on the field oxide, the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the component comprising an adhesion layer formed on the field oxide and a conductive silicide layer formed on the adhesion layer.

28. (Four Times Amended) A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof, the trench extending into the substrate substantially perpendicularly to the surface of the substrate;

a field oxide in the trench, the field oxide having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the substantially straight sides extending from the trench beyond the surface of the substrate and above any adjacent structures on the upper surface of the substrate, the substantially straight sides extending substantially perpendicularly to the surface of the substrate and not extending laterally from the trench over the surface of the substrate; and

a gate structure formed on the substrate, the gate structure extending from the [field oxide]upper surface of the substrate by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the field oxide not contacting any portion of the gate structure.

30. (Four Times Amended) A microelectronic device, comprising:

a microelectronic substrate having a recess formed in a surface thereof, the recess extending into the substrate substantially perpendicularly to the surface of the substrate; and

a field oxide deposited in the recess, the field oxide having sides that are substantially straight and substantially parallel from a bottom of the recess to a top surface of the field oxide, the substantially straight sides extending substantially perpendicularly to the surface of the substrate from the recess and beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of a component formed on the field oxide, the field oxide not extending laterally from the recess over the surface of the substrate, and the field oxide extending above adjacent structures on the upper surface of the substrate.

32. (Five Times Amended) A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a gate structure formed on the substrate, the gate structure including a gate oxide layer formed on the microelectronic substrate, a first gate layer formed on the gate oxide layer, an adhesion layer formed on the first gate layer, and a conductive layer formed on the adhesion layer; and

a field oxide deposited in the trench, the field oxide extending substantially perpendicularly to the surface of the substrate from the trench beyond the surface of the substrate and above adjacent structures on the upper surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate, the field oxide having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the substantially straight sides not contacting the gate oxide layer and not extending laterally from the recess over the surface of the substrate.

34. (Four Times Amended) A microelectronic device, comprising:

a microelectronic substrate having a surface with a trench formed therein;

a field oxide within the trench and having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the substantially straight sides projecting therefrom substantially perpendicularly to the surface of

the substrate and above adjacent structures on the upper surface of the substrate by a height which is small enough to prevent the formation of spacers adjacent the field oxide, the field oxide not extending laterally from the trench over the surface of the substrate; and

a component formed on the field oxide.

-- 38. (New) The microelectronic device of claim 22 wherein a first distance measured from the top surface of the field oxide layer to the level of the upper surface of the substrate is up to one half of a second distance measured from the level of the upper surface of the substrate to the upper surface of the gate structure.

39. (New) The microelectronic device of claim 26, further comprising a gate structure including a gate oxide layer formed on the upper surface of the substrate, the gate structure extending from the upper surface of the substrate to a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the field oxide not contacting any portion of the gate structure.

40. (New) The microelectronic device of claim 26 wherein the silicide layer comprises tungsten silicide.

41. (New) The microelectronic device of claim 26, further comprising a thin layer of oxide formed on the silicide layer.

42. (New) The microelectronic device of claim 30 further comprising a gate structure including a gate oxide layer formed on the upper surface of the substrate, the gate structure extending from the upper surface of the substrate to a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the field oxide not contacting any portion of the gate structure.

43. (New) The microelectronic device of claim 34, further comprising a gate structure including a gate oxide layer formed on the upper surface of the substrate, the gate

structure extending from the upper surface of the substrate to a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the field oxide not contacting any portion of the gate structure. --